

AMENDMENTS TO THE DRAWINGS

The attached sheet of drawing includes changes to Fig. 22. Fig. 22, is labeled PRIOR ART.

Attachment: Replacement sheet

REMARKS

In response to the Office Action dated April 19, 2006, claims 1, 8, 14 and 15 are amended, and claims 17 and 18 are added. Claims 1-18 are now active in this application. No new matter has been added.

The indication that claims 6 and 16 are objected to, but would be allowable if rewritten in independent form including all the limitations of the base claim and any intervening claims is acknowledged and appreciated.

Claims 14 and 15 have been amended to delete "and" from line 6 to provide better form.

REJECTION OF CLAIMS UNDER NONSTATUTORY DOUBLE PATENTING

Claims 1, 2, 8, 9 and 10 have been provisionally rejected on the ground of non-statutory obviousness-type double patenting as being unpatentable over claims 1, 9 and 10, respectively, of co-pending Application No. 10/505,433 in view of Yoshikawa (USPN 6,335,554).

However, independent claim 1 has been amended and is now patentable over Yoshikawa. Consequently, withdrawal of the provisional rejection of independent claim 1 and dependent claims 2, 8, 9 and 10 on the ground of non-statutory obviousness-type double patenting is respectfully solicited.

REJECTION OF CLAIMS UNDER 35 U.S.C. § 102 AND § 103

I. Claims 1-5 and 8-15 has been rejected under 35 U.S.C. § 102(b) as being anticipated by Yoshikawa (USPN 6,335,554).

Claim 7 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over Yoshikawa. The Examiner contends that Yoshikawa discloses all the limitations of the claim except for the gate length of the gate electrode being between 0.015 μm and 0.5 μm . The Examiner refers to Fujiwara (U.S. 2002/0097621) as disclosing use of the gate length of 90 nm to reduce the threshold voltage and asserts that it would have been obvious to one having ordinary skill in the art to use the gate length of 90 nm in order to reduce the threshold of the threshold voltage.

As the Examiner refers to Fujiwara as disclosing use of the gate length of 90 nm to reduce the threshold voltage, it is presumed that the Examiner intended that claim 7 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Yoshikawa in view of Fujiwara.

II. To expedite prosecution, independent claim 1 has been amended to recite, *inter alia*:

...wherein

...

the second conductivity type diffusion layer regions are respectively offset relative to edges of the single gate electrode,

no electrode exists on each of the two charge holding portions, and

the two charge holding portions are respectively located above part of the channel region and part of each of the second conductivity type diffusion layer regions.

Yoshikawa (USPN 6,335,554)

Yoshikawa teaches two gate electrodes 3 and 8, but not a single electrode as apparent from Fig. 1. Furthermore, the gate electrodes 8 are positioned on the charge holding portions 4a and 4b, as shown in Fig. 1.

In contrast, amended independent claim 1 has only a single gate electrode 13, and no electrodes exists on the charge holding portions 61, 62, as shown in Fig. 1.

Sakagami et al. (USPN 5,838,041), cited in the IDS filed September 2, 2004

The right side charge holding portions 19 of Sakagami et al. are not formed on a part of the channel region, but all on the diffusion layer regions 16, 20, as shown in Fig. 2.

In contrast, part of the charge holding portions 61, 62 of amended independent claim 1 are respectively located on a part of the channel region, as shown in Fig. 1.

III. None of the cited prior art references disclose the features now recited in amended independent claim 1. Consequently, amended independent claim 1 is patentable over Yoshikawa, as are claims 2-7 and 14-16 depending from amended independent claim 1, even when considered in view of Fujiwara (U.S. 2002/0097621). Therefore, the allowance of claims 1-7 and 14-16, as amended, is respectfully solicited.

NEW CLAIMS

New independent claims 17 and 18 are submitted. Claim 17 recites, *inter alia*:

A semiconductor storage device comprising:

...

wherein

...

the first conductivity type is P type,

the second conductivity type is N type,

the carriers are positive holes,

the first voltage is higher than the reference voltage,

the second voltage is lower than the reference voltage, and

the third voltage is higher than the reference voltage.

Claim 18 is similar to claim 17, but recites, *inter alia*:

A semiconductor storage device comprising:

...

wherein

...

the first conductivity type is N type,

the second conductivity type is P type,

the carriers are electrons,

the first voltage is lower than the reference voltage,

the second voltage is higher than the reference voltage, and

the third voltage is lower than the reference voltage.

The above noted features recited in new claims 17 and 18 are recited also in dependent claims 14 and 15, respectively, and are not disclosed or suggested in the cited references. Therefore, the allowance of new independent claims 17 and 18 is respectfully solicited also.

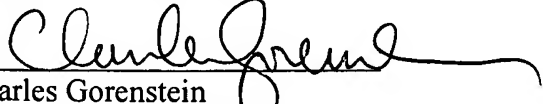
CONCLUSION

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Edward J. Wise (Reg. No. 34,523) at the telephone number of the undersigned below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Dated: August 21, 2006

Respectfully submitted,

By 

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Attachment: Replacement Drawing (Fig. 22)


CG/EJW/vd